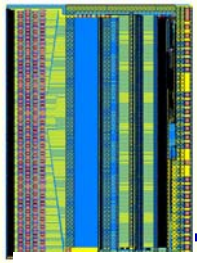
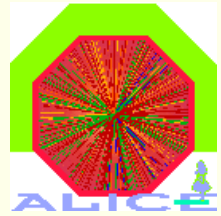


FMD – Forward Multiplicity Detector

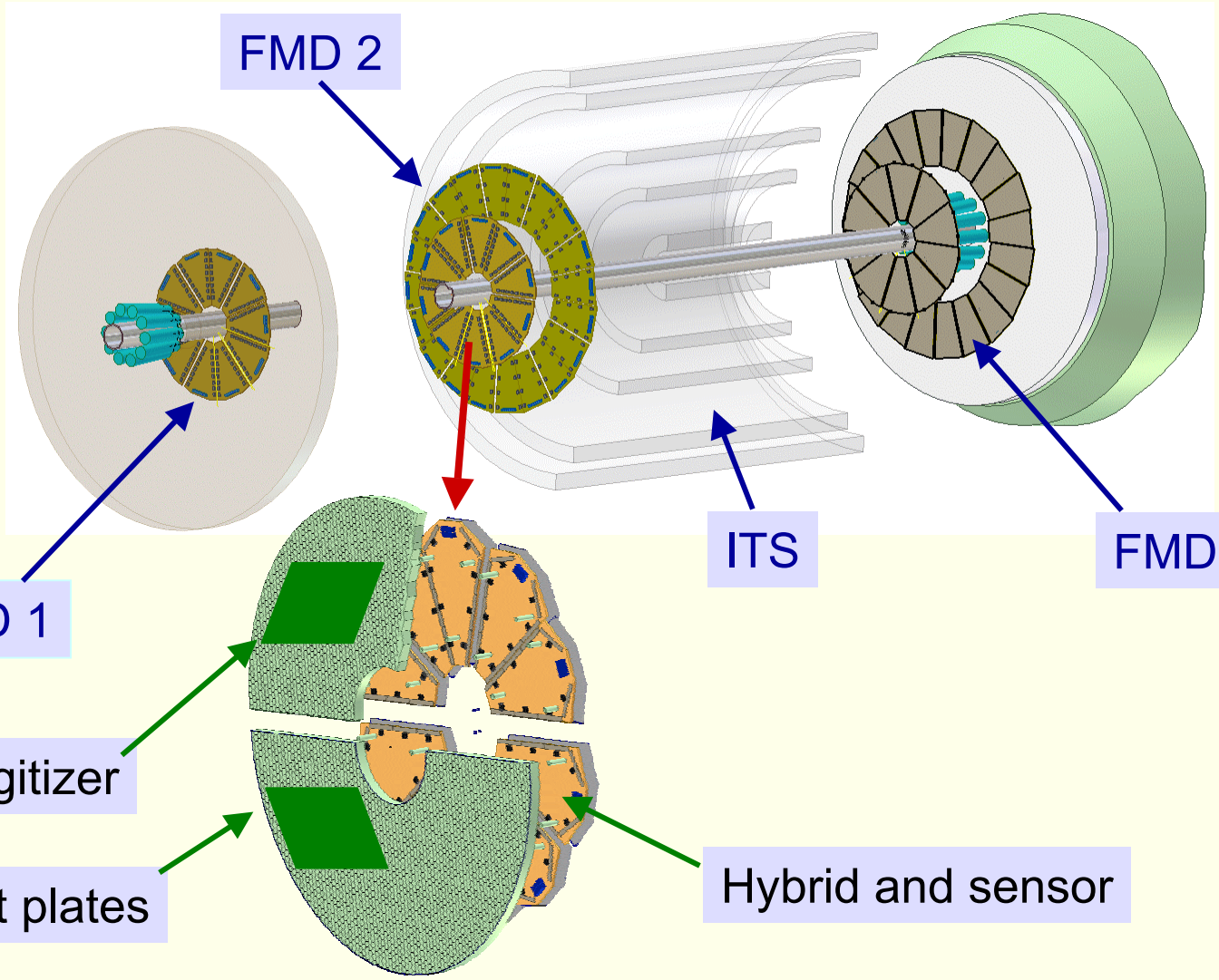


ALICE Meeting on Rad. Tolerant Electronics
CERN, 30 August 2004

Børge Svane Nielsen
Henrik Bertelsen
Niels Bohr Institute

1. Silicon strip sensors: Hamamatsu
2. Preamp-shaper chips: VA1_ALICE in production
3. Hybrids: VA1_ALICE with passive components
4. FMD Digitiser Card: Design based on TPC FEC and ”known” VA1 read-out protocol
5. Read-out and Controls: TPC RCU

Five FMD Rings



Radiation environment

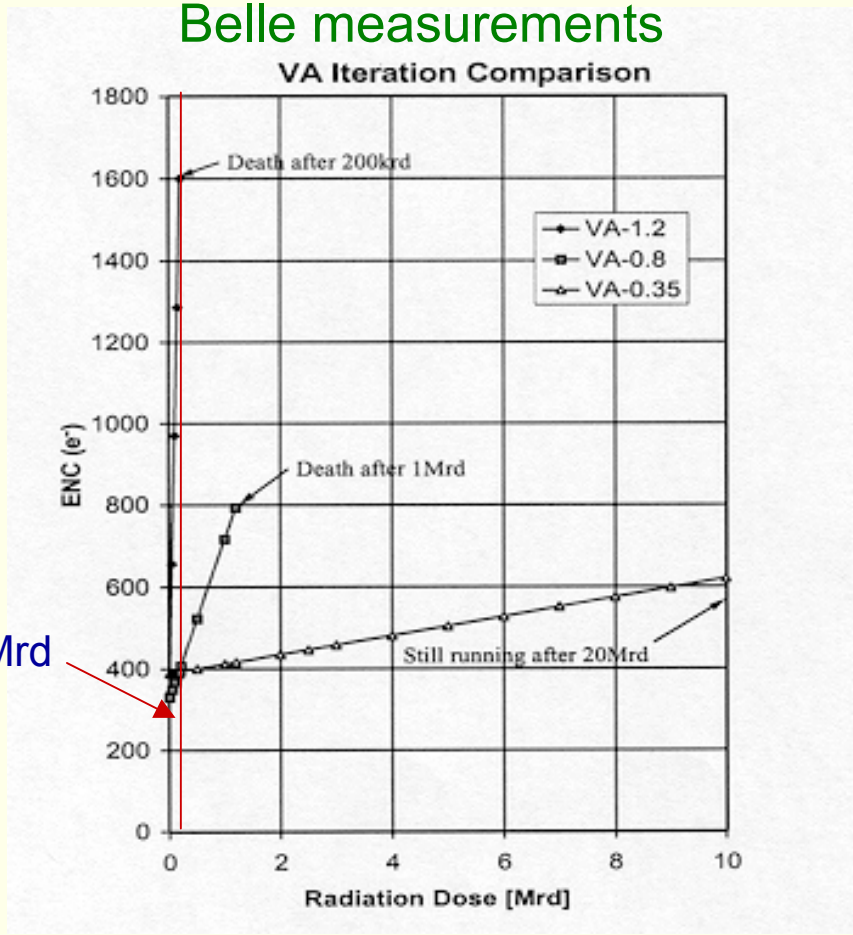
Doses and Fluences in Central ALICE (10 years running):

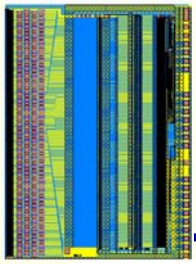
Doses in FMD:

	Dose [Gy]	h-Φ [cm**-2]
FMD3	80-1350	9-14 E+11
FMD2	40-2300	1.4-6.5 E+11
FMD1	900-3300	2.5-5.6 E+11

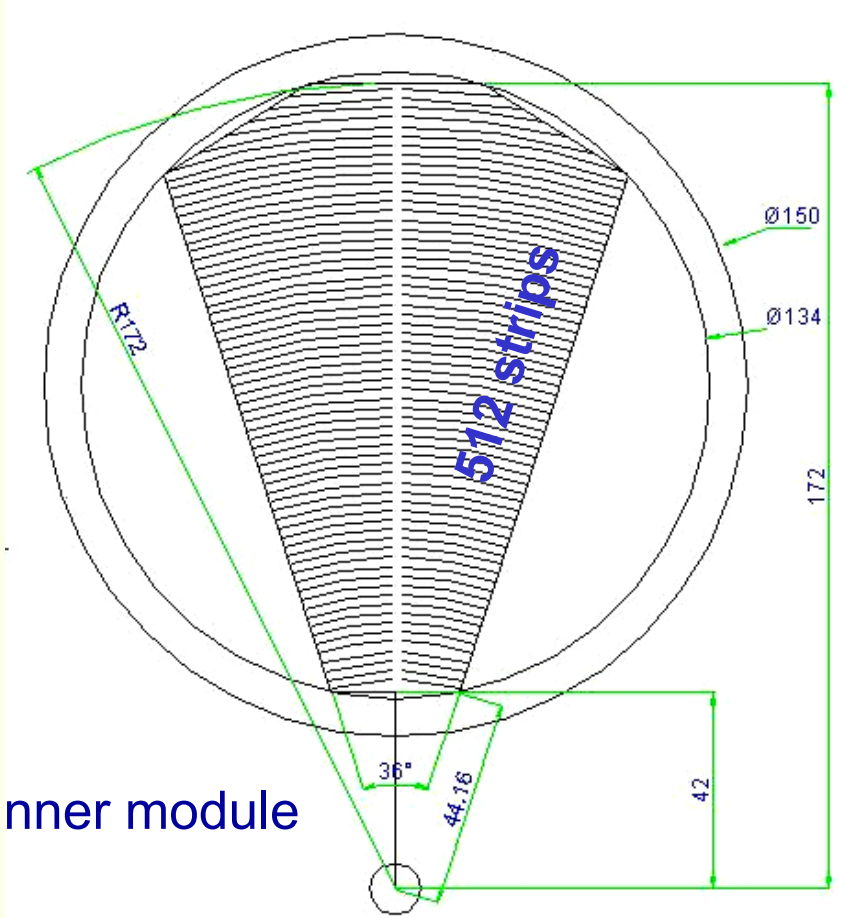
=0.33 Mrd

Belle measurements

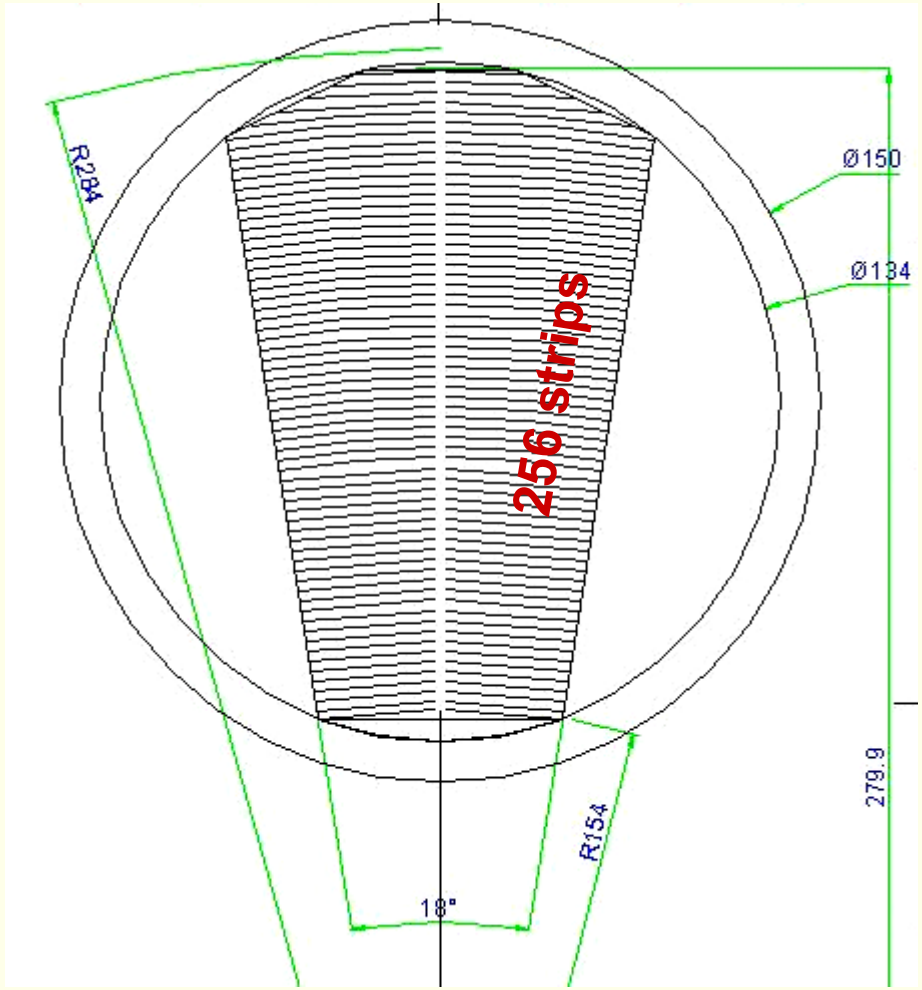




FMD sensors



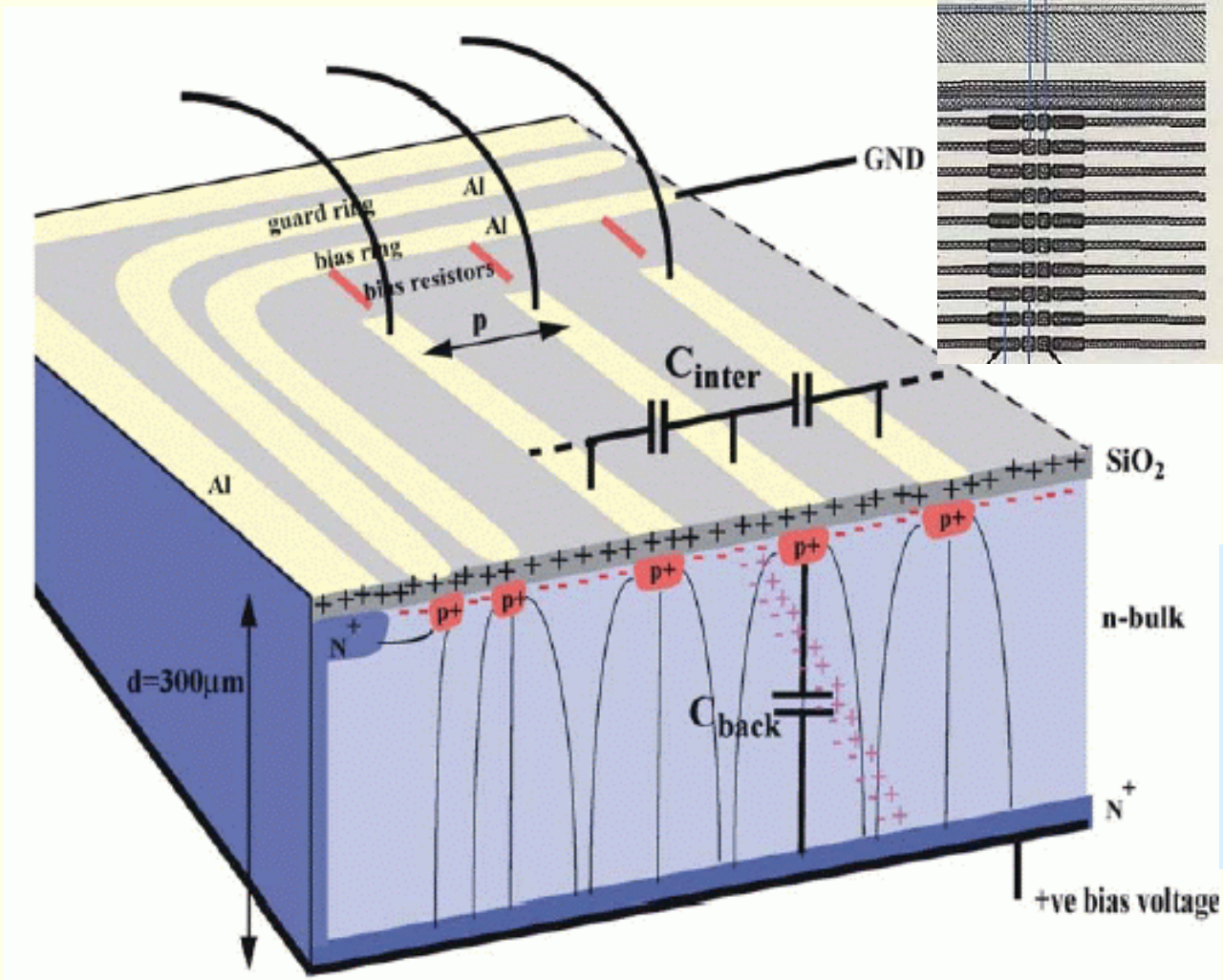
Inner module

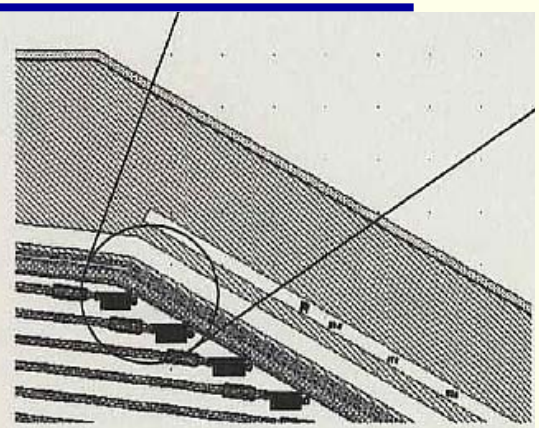


Outer module

Si strip sensors from 6” wafers.
Manufactured by Hamamatsu.

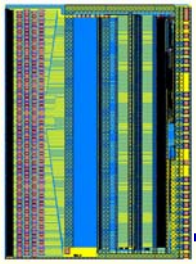
Sensor design



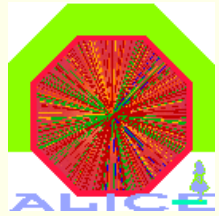


Design very similar to CMS sensor, except:

- geometry
- "standard" ~ 5kΩcm high resistivity silicon



Read-out and Controls



ON DETECTOR

NEAR PATCH PANEL

IN COUNTING ROOM

FMD Module

FMD Digitizer

RCU

Front-end bus ~ 3 m

Analog serial link (10 MHz) ≤ 0.5 m

× 16

ALTRO (16 ch)

ALTRO (16 ch)

ALTRO (16 ch)

Read-out CTRL

VA

VA read-out control

Bus controller (conf. & R/O)

Data Proc. and Memory

Local Monitor and Control

BOARD controller

DAQ int. (DDL-SIU)

DCS int. (Ethernet)

Trigger int. (TTC-rx)

DDL

DCS

TTC optical Link

(Clock, L1 and L2)

Control Network (I²C-serial link)

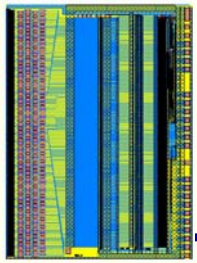
Trigger L0

1 ring: 10/20 modules
Full FMD: 70 modules

2 Digitizers
10 Digitizers

1 RCU per ring system
3 RCU's

BSN, 17 Feb 2004

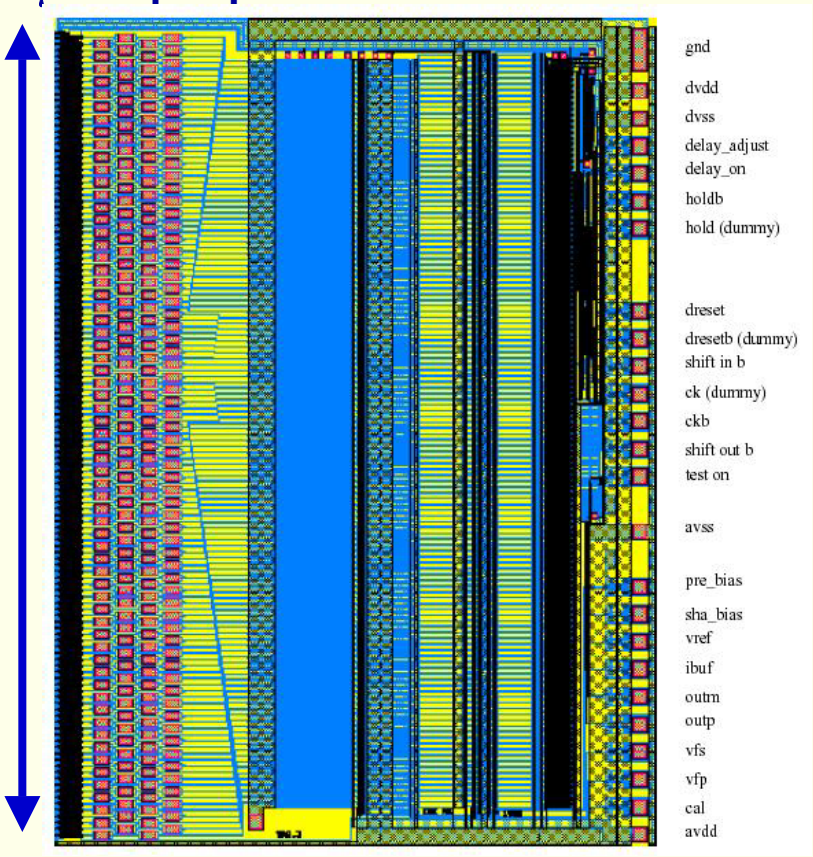


Custom preamp-shaper chip: VA1_ALICE in production

VA1_ALICE

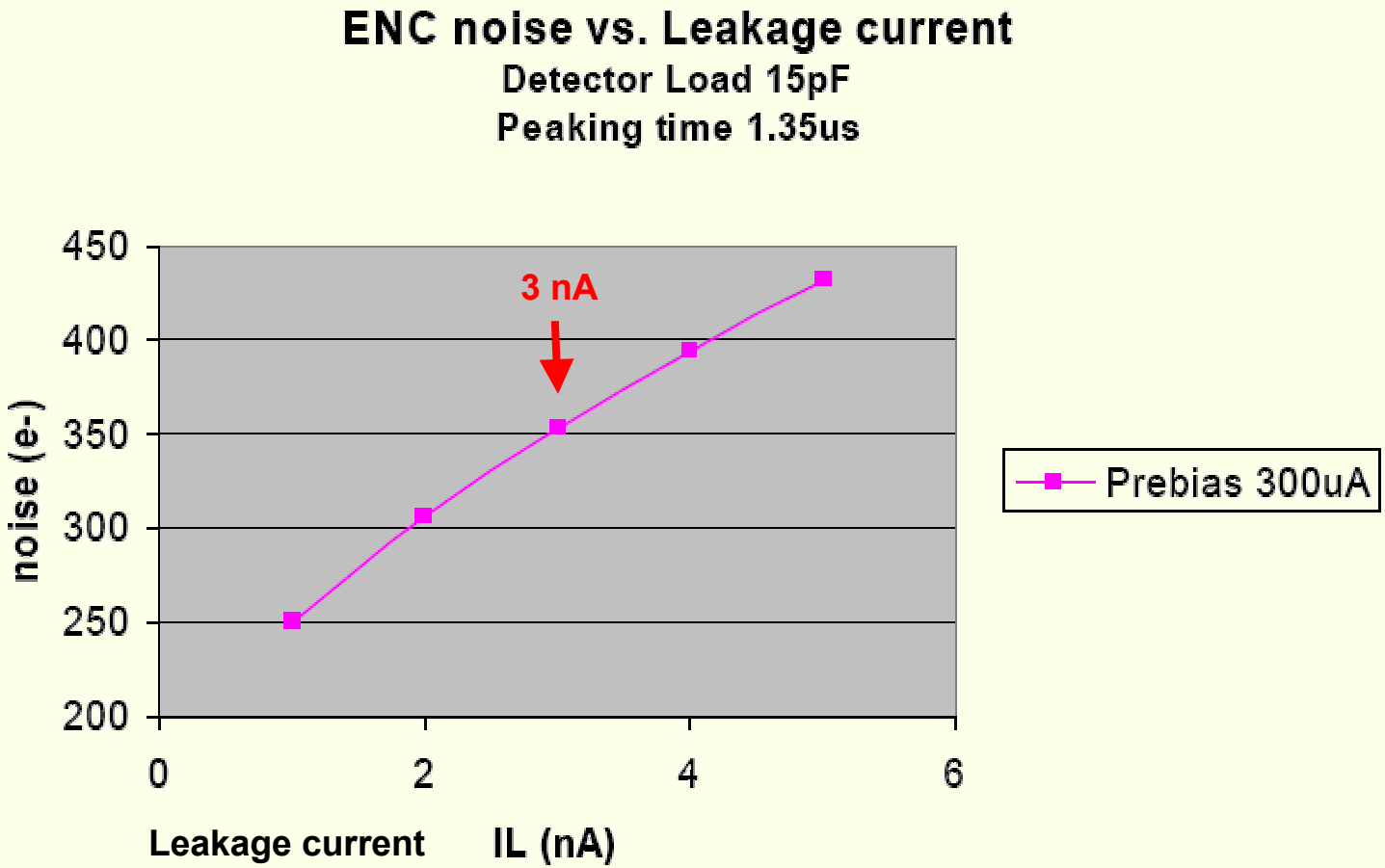
a VA1 in 0.35 μm technology

45 μm input pitch



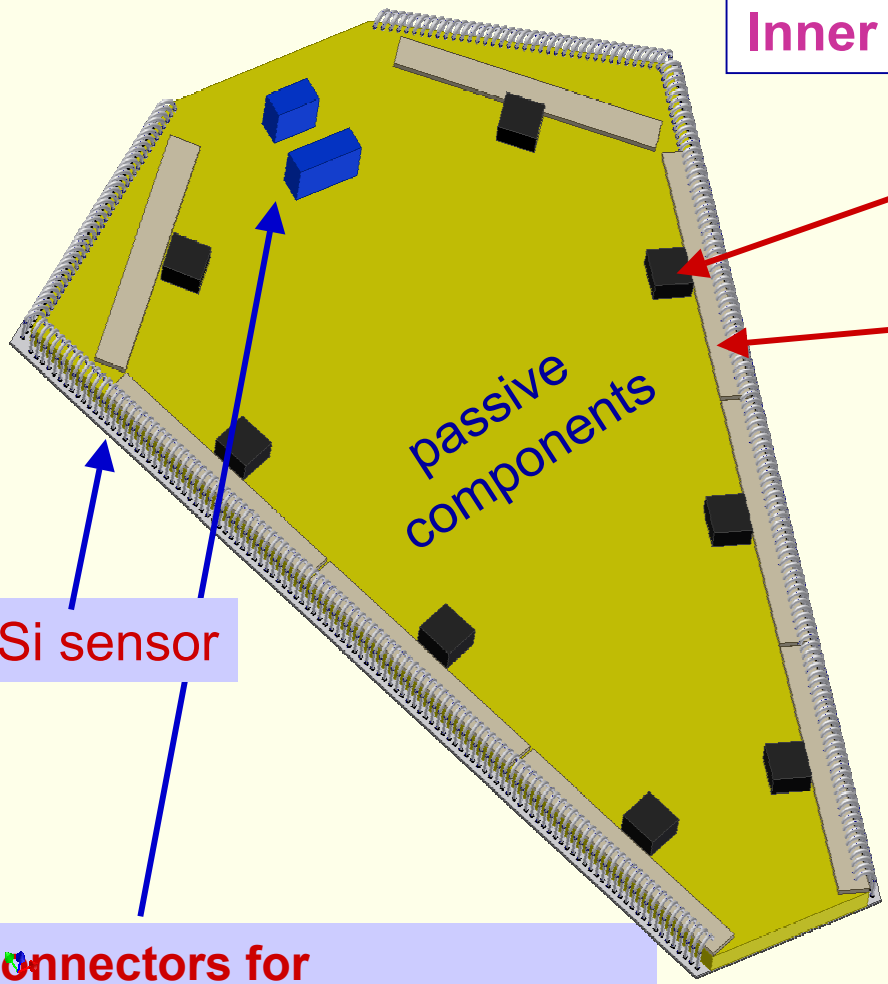
Radiation hardness	> 500-1000 krad
Peaking time	1.2-1.5 μsec (optimised at 1.35 μsec)
Noise (ENC)	< 500 e- (= 0.02 MIP)
Capacitance matching	5-25 pF
Dynamic range	0-20 MIPs (or ±10 MIPS)
Highly integrated	128 channels per chip
Read-out speed	~ 10 MHz
Test and calibration circuits	included
Power consumption	0.8 mW per channel
Compatibility with ALTRO	requires level shift
Early prototype	VA1' useful
Affordable cost	yes
Channel count	51,200 (400 chips à 128 channels)

VA1_ALICE noise simulations



Hybrids

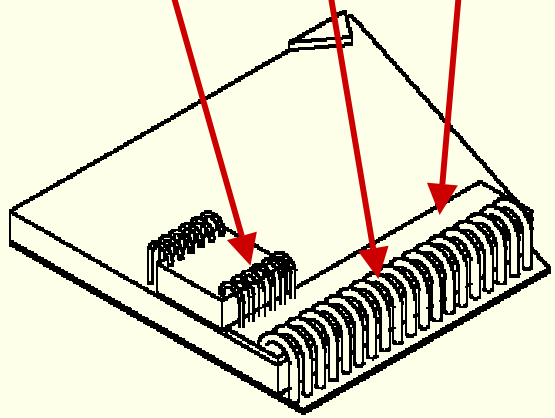
Inner module



VA1_ALICE (128 channels)

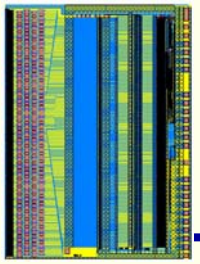
pitch adapter (ceramics)

bonding

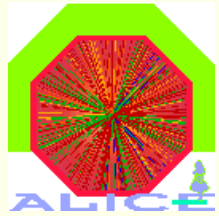


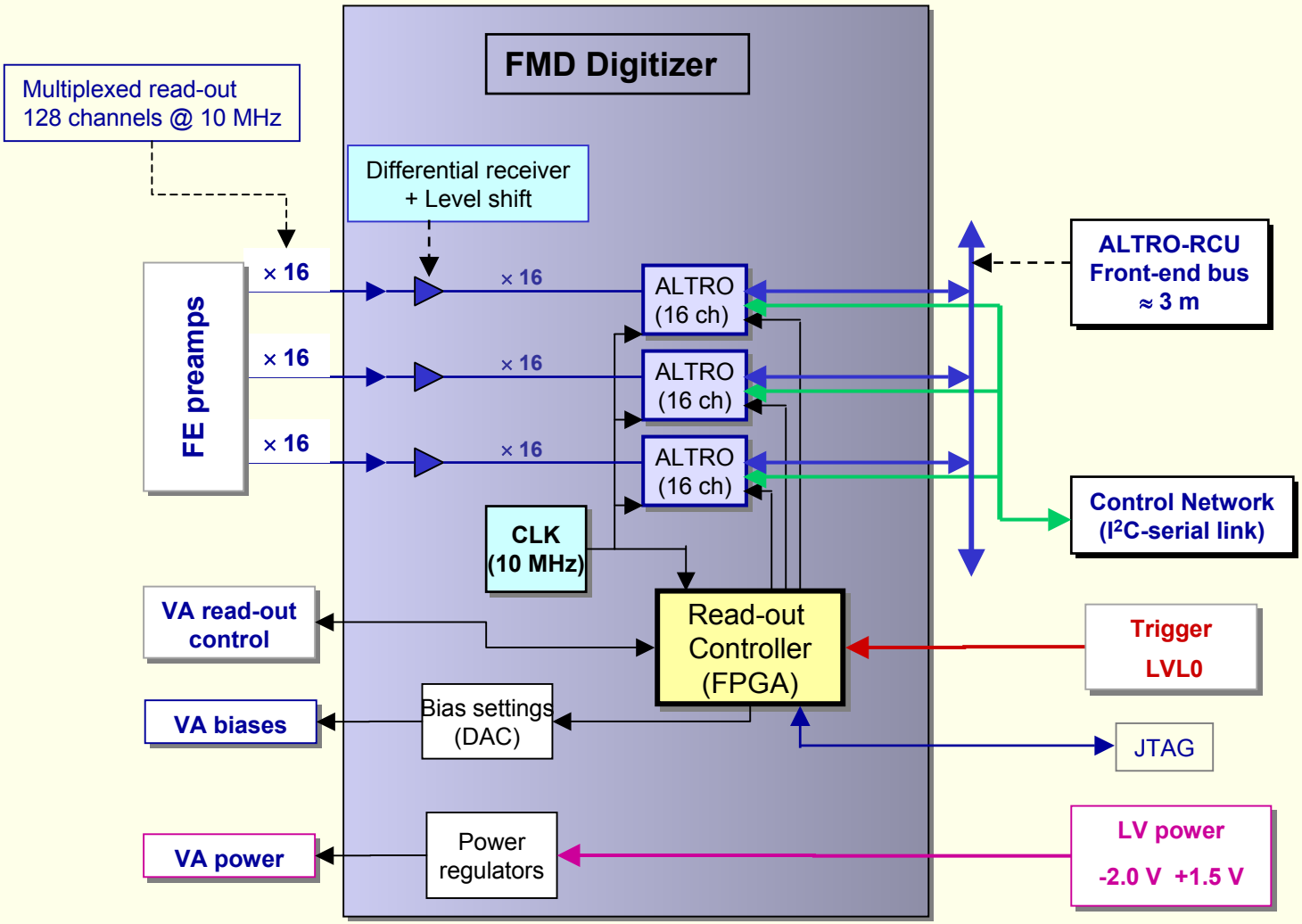
Si sensor

Connectors for
power, control, read-out, bias

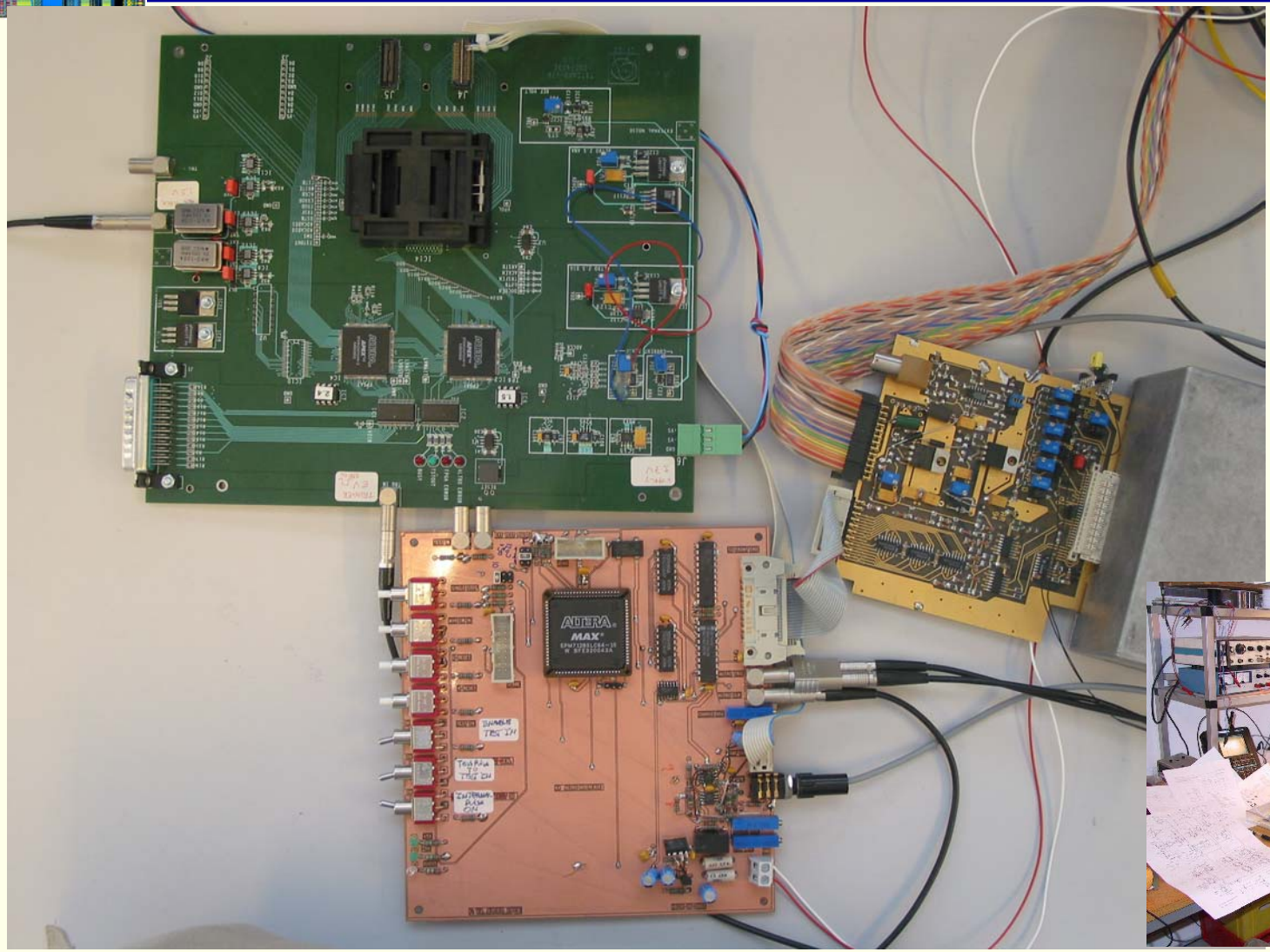


FMD Digitizer

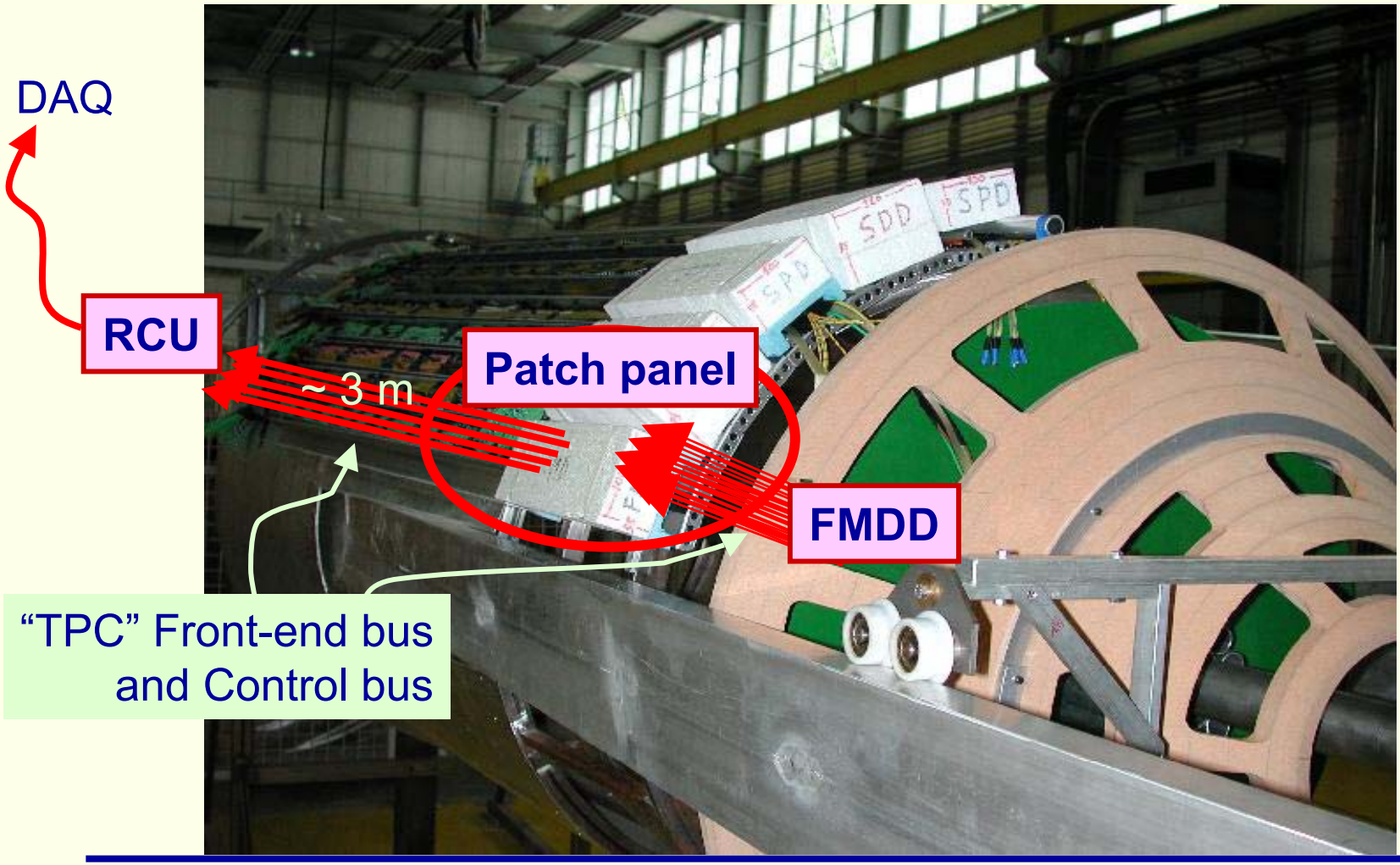




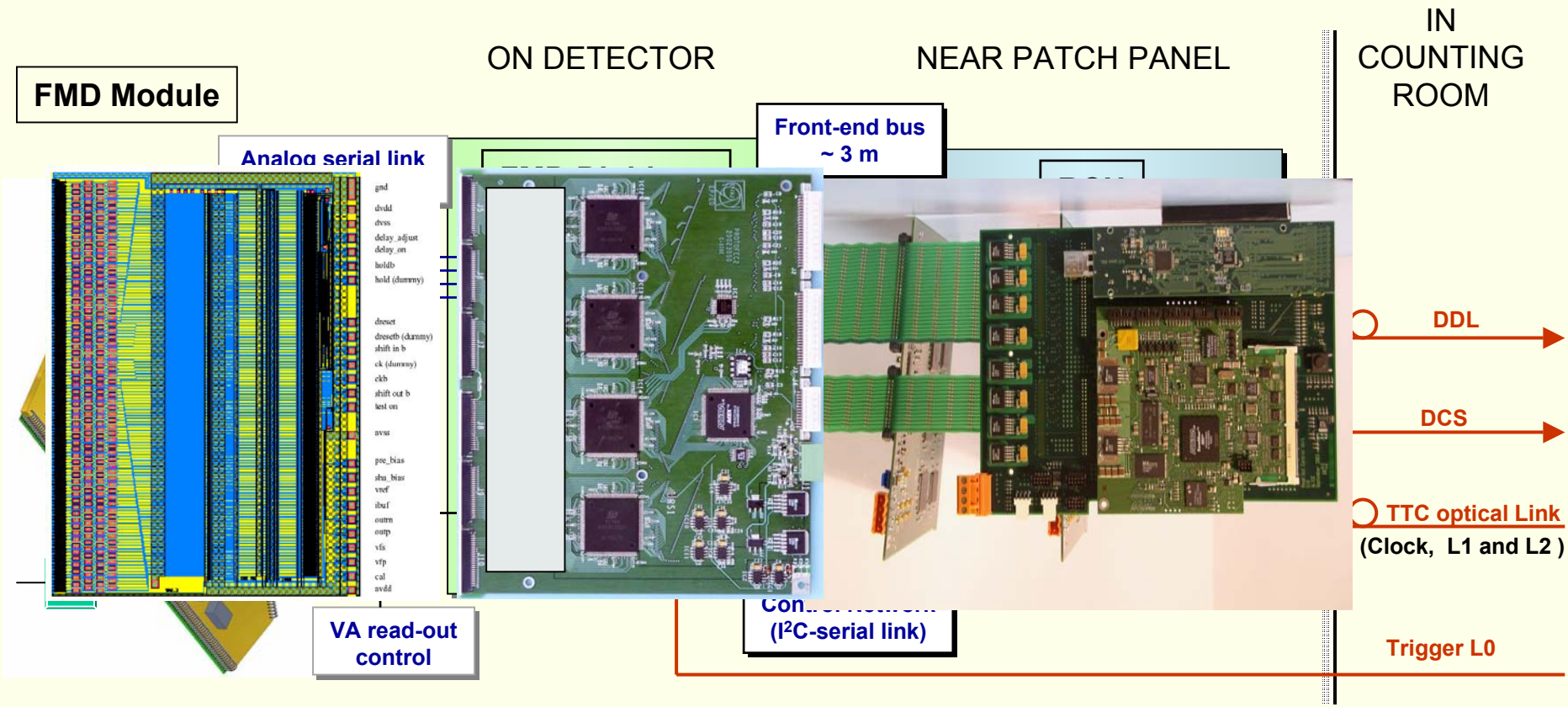
FMDD study set-up



RCU location



Read-Out modules



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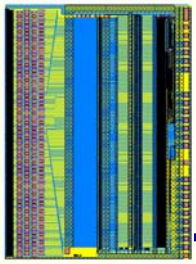
Full FMD: 70 modules

2 Digitizers
10 Digitizers

1 RCU per ring system
3 RCU's

BSN, 17 Feb 2004



Summary

Electronics components of FMD:

- Preamp-shaper-multiplexer on hybrid:
  VA1_ALICE in 0.35 μm technology by IDEAS, Oslo
  Rad.level 200-3300 Gy

- FMD Digitizer: use ALTROs and TPC FEC schematics
  + VA1 read-out protocol with common 10 MHz clock,
  to be built at NBI, Copenhagen
  Need to be aware of higher rad. levels than at TPC
  Rad.level 100-1000 Gy

- RCU identical to the one from TPC and PHOS
  Rad.level 10-100 Gy