NBI

Si-FMD electronics

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Issues in defining front-end electronics specs

Si-detector characteristics:

Channels per sector	32	64	**128**	256	512
Strip areas [cm^2]	0.8–3.7	0.4–1.8	**0.2–0.9**	0.1–0.5	0.05–0.23
Strip capacitances [pF]	32–131	19–66	**12–36**	8–22	7–13
Occupancies [# particles/strip]	4–22	2–11	**1–5**	0.6–3	0.3–1.3

Detector capacitance $\approx 34\mathrm{pF}/\mathrm{cm}^2 + 5\mathrm{pF}$
For 300 μm Silicon: 1 mip = 3.6 fC = 22,400 e^-

ALICE trigger timings:

– Level 0: 0.9–1.2 μs, pipeline running at 25/125 ns
– Level 1: 5.2 μs
– Level 2: 88 μs

Main front-end electronics issues:

- match input *capacitance* of preamplifier circuit
- match preamplifier *noise* and *dynamic range* to Si signal amplitude
- match *shaping time* and *read-out* to ALICE timing
- participation in *trigger* decision?
- match channel count and layout to detector
- radiation tolerance
- cost and availability

Front-end chips

Survey of some existing front-end chips

Front-end chip	VA1_prime	HAL25	VA_Rich	Si-FMD Specs
Experiment	BELLE SVD	ALICE SSD		
Peaking time	0.3-1 μs	1.2-2.2 μs	1-3 μs	1-2 μs
Channels/chip	128	128	32	32, 64, 128
Dynamic range	$\pm$ 10 mips	$\pm$ 14 mips	$\pm$ 20 mips	0-50 mips
	0-20 mips		0-40 mips	
Input capacitance	large	$<$ 20 pF	10-30 pF	10-40 pF
Noise	180e+7.5e/pF	207e+10e/pF	100e+15e/pF	
@ 36 pF	450 e$^-$	567 e$^-$	640 e$^-$	$< 2000e^-$
Memory/pipe	1 event S/H	1 event S/H	1 event S/H	
Read-out	analog/serial	analog/serial	analog/serial	analog/digital
Read-out time	10 MHz	10 MHz	10 MHz	5-10 MHz
Trigger on chip	no	no	no	no
Trigger off chip	L2	L2	L2	
Technology	0.35 μ AMS	0.25 μ IBM	1.2 μ AMS	
Rad. hard	$\geq$ 1 Mrad	$\geq$ 1 Mrad	$\approx$ 50 krad	$\geq$ 200 krad

Existing front-end candidates do not meet all requirements:

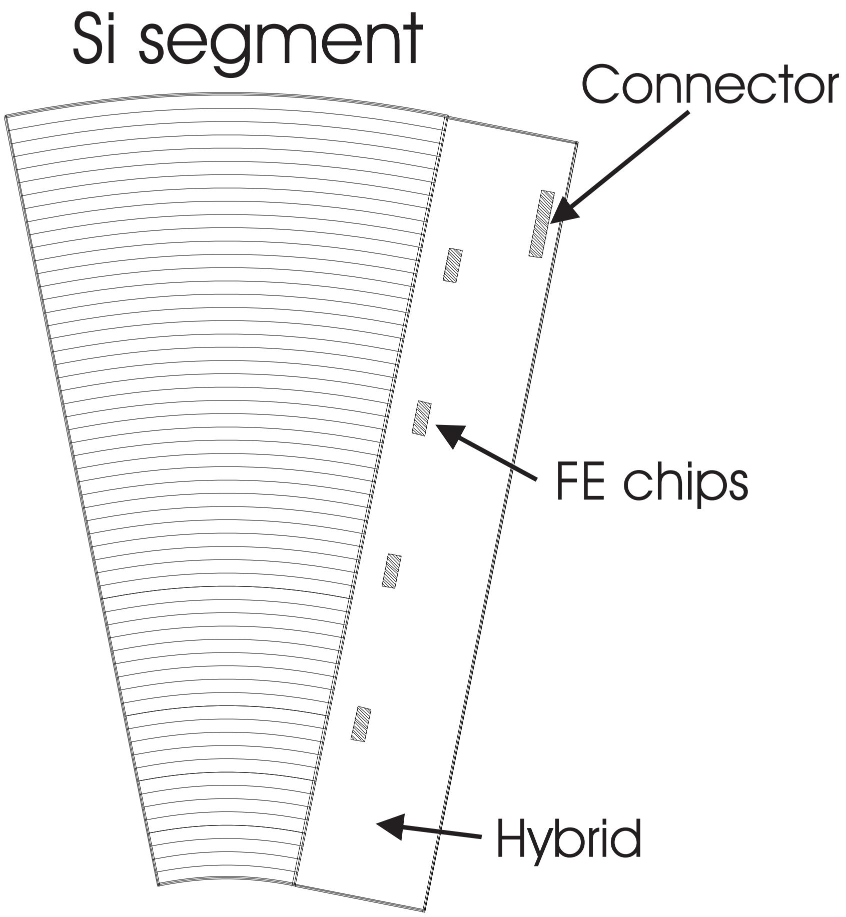
- HAL25:
  - low dynamic range: need ≥ 512 channels/sector
  - low capacitance: need ≥ 256 channels/sector
  - too long time constant on Preamp $\Longrightarrow$ *rate limitation* (tbv)
- VA1_prime:
  - too low dynamic range
- VA_Rich:
  - slightly too low dynamic range
  - not radiation hard

VA can easily be modified. Larger modification to include analog sum for triggering.

Hybrids

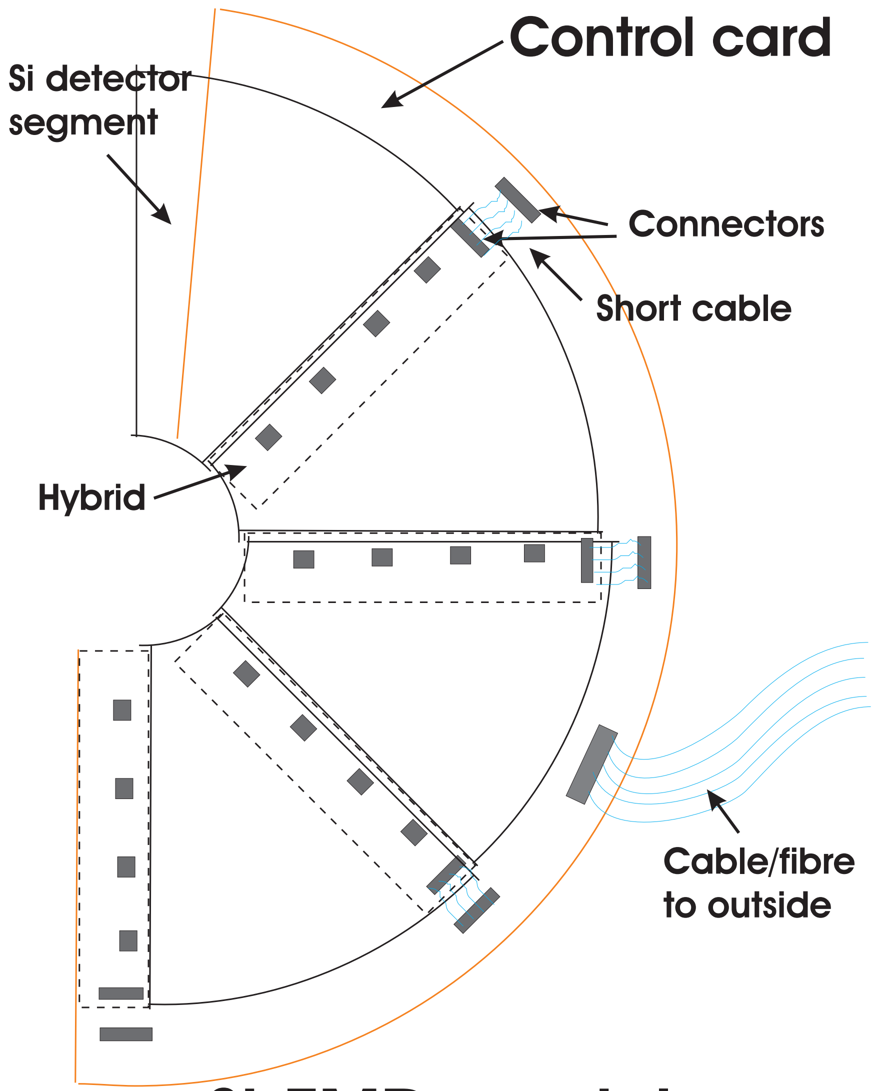
Suggest elongated hybrid along long side of Si detector:

– Mechanical support of Si detector
– Bonding pads
– FE amplifier/trigger chips
– Passive components for signal and power distribution
– Driver for output signal
– High voltage
– Monitoring (temperatures, voltages)
– Cable connector for data read-out, chip controls and high voltage.



Mechanical layout, cables, back-end

Sketch of possible Si-FMD assembly with control/receiver/repeater system on card right behind detector.



Si-FMD module

— or all controls on hybrids and daisy-chain of cables between segments.

Segmentation in ϕ

Outer rings based on 15° strips, i.e. only η segmentation on each wafer.

Inner rings based on 36° detector segments
Should be divided into 2 (or more?) strip segments in ϕ.
Tab bonded flat cable to connect to hybrid?

Cables.

– Short cables between segments or from segments to control card.

– One long signal/control cable out per module (half disk).

– Individual HV cables out

Back-end.

– HV modules.

– Receiver modules under computer control (VME?):
ADC, clocks, sequencer for read-out
low voltage supplies
control and monitoring of FE electronics
calibration and testing

– DAQ interface module.

Summary

Not much concrete progress this summer, but some issues seem clearer:

– need final decision on trigger/no trigger
– segmentation/strip layout still not final.

Preferred electronics solution is based on the IDEAS company.

– IDEAS can modify the classic Viking (VA) preamp/shaper chips in radiation tolerant technology (0.8 μm AMS verified to 1 Mrad or 0.35 μm AMS verified to 20 Mrad).

– chips are adaptable to our detector specifications (with e.g. 128 or 256 channels/sector).

– modifications possible to include analog trigger sum for L1 triggering.

– IDEAS can design and produce tested hybrids.

– IDEAS can bond Si wafers to hybrids, deliver fully tested system.

– Lab test systems available.

– We need to work on control and back-end electronics.

– First cost estimates seem OK, but we need to design concrete case.