NBI

Tentative proposals for Si-FMD electronics

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Issues in defining front-end electronics specs

Si-detector characteristics:

Channels per sector	32	64	**128**	256	512
Strip areas [cm^2]	0.8–3.7	0.4–1.8	**0.2–0.9**	0.1–0.5	0.05–0.23
Strip capacitances [pF]	32–131	19–66	**12–36**	8–22	7–13
Occupancies [# particles/strip]	4–22	2–11	**1–5**	0.6–3	0.3–1.3

Detector capacitance $\approx 34\mathrm{pF}/\mathrm{cm}^2 + 5\mathrm{pF}$
For 300 μm Silicon: 1 mip = 3.6 fC = 22,400 e^-

ALICE trigger timings:

– Level 0: 0.9–1.2 μs, pipeline running at 25/125 ns
– Level 1: 5.2 μs
– Level 2: 88 μs

Main front-end electronics issues:

- match input *capacitance* of preamplifier circuit
- match preamplifier *noise* and *dynamic range* to Si signal amplitude
- match *shaping time* and *read-out* to ALICE timing
- participation in *trigger* decision?
- match channel count and layout to detector
- radiation tolerance
- cost and availability

First specs for the front-end electronics

Assuming 128 Si strips per sector:

— Highly integrated ASIC (32, 64 or 128 channels per chip)
— Peaking time: $1 - 2\mu$s
Note: in p+p, L=3×10^{30} *implies 5* μs *between events on average while L=*5×10^{31} *implies 0.2* μs *between events on average*
— Noise: ≤ 0.1 mips (2,200 e^-)
— Input capacitance: 10-40 pF
— Dynamic range: $0 - 50$ or more
— On-chip Sample/Hold and serial read-out
— Either: Fast, parallel read-out and on-hybrid trigger chip
Or: On-chip analog trigger sum and/or discriminator
— Radiation hard: ≥ 200krad
— Test and calibration circuits
— Compatible with ALICE slow controls + trigger + DAQ
— Early version for Si detector testing
— Affordable costs

Front-end chips

Survey of some existing front-end chips

Front-end chip	VA1_prime	HAL25	VA_Rich	Si-FMD Specs
Experiment	BELLE SVD	ALICE SSD		
Peaking time	0.3-1 μs	1.2-2.2 μs	1-3 μs	1-2 μs
Channels/chip	128	128	32	32, 64, 128
Dynamic range	$\pm$ 10 mips	$\pm$ 14 mips	$\pm$ 20 mips	0-50 mips
	0-20 mips		0-40 mips	
Input capacitance	large	$<$ 20 pF	10-30 pF	10-40 pF
Noise	180e+7.5e/pF	207e+10e/pF	100e+15e/pF	
@ 36 pF	450 e$^-$	567 e$^-$	640 e$^-$	$< 2000e^-$
Memory/pipe	1 event S/H	1 event S/H	1 event S/H	
Read-out	analog/serial	analog/serial	analog/serial	analog/digital
Read-out time	10 MHz	10 MHz	10 MHz	5-10 MHz
Trigger on chip	no	no	no	yes
Trigger off chip	L2	L2	L2	
Technology	0.35 μ AMS	0.25 μ IBM	1.2 μ AMS	
Rad. hard	$\geq$ 1 Mrad	$\geq$ 1 Mrad	$\approx$ 50 krad	$\geq$ 200 krad

Existing front-end candidates do not meet requirements:

- HAL25:
  - low dynamic range: need ≥ 512 channels/sector
  - low capacitance: need ≥ 256 channels/sector
  - L1 trigger not possible
- VA1_prime:
  - too low dynamic range
  - L1 trigger not possible
- VA_Rich:
  - slightly too low dynamic range
  - L1 trigger not possible
  - not radiation hard

The VA architecture classic for Si detectors. It is used by both BELLE SVD and PHOBOS (RHIC), and many older experiments (DELPHI, ...).

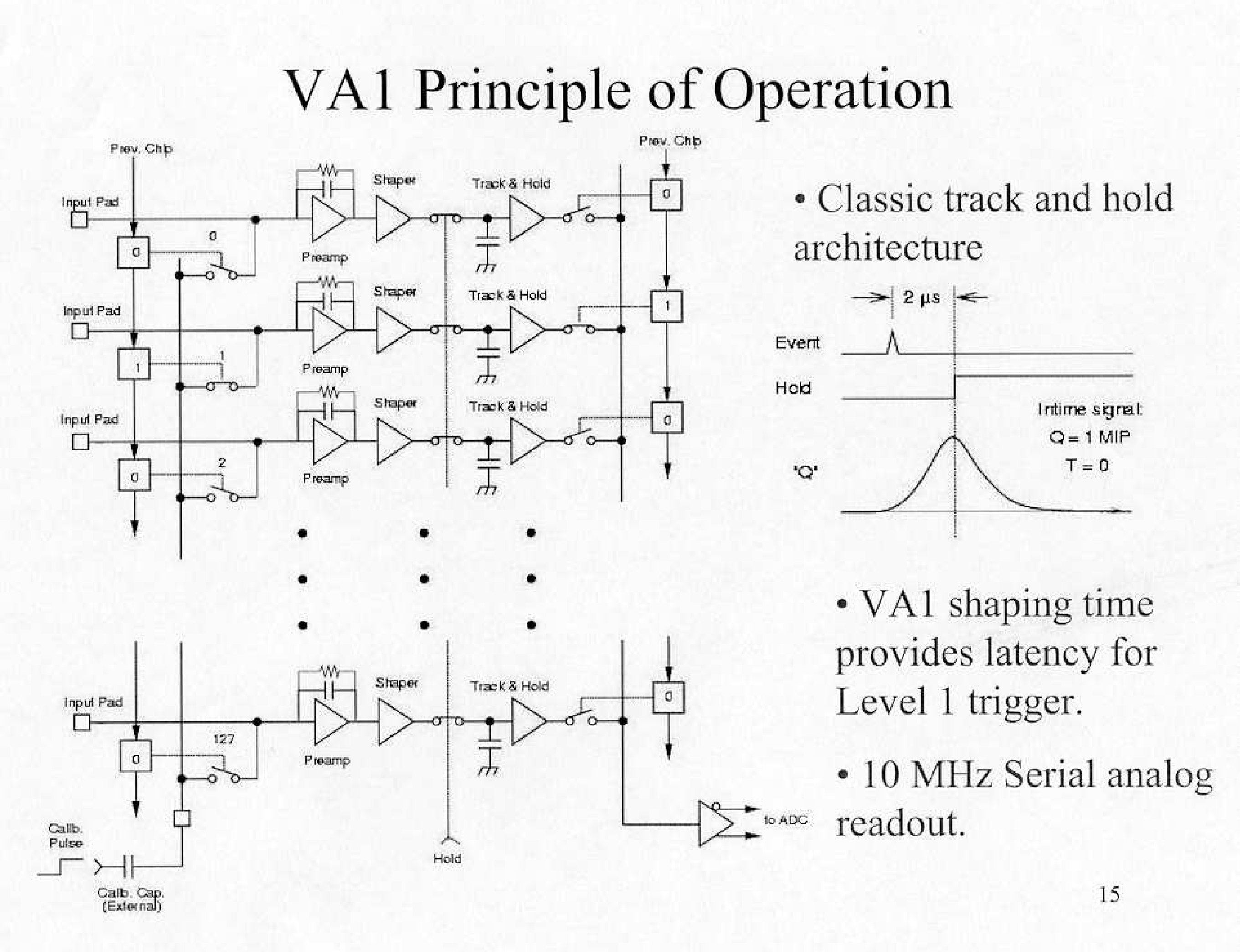


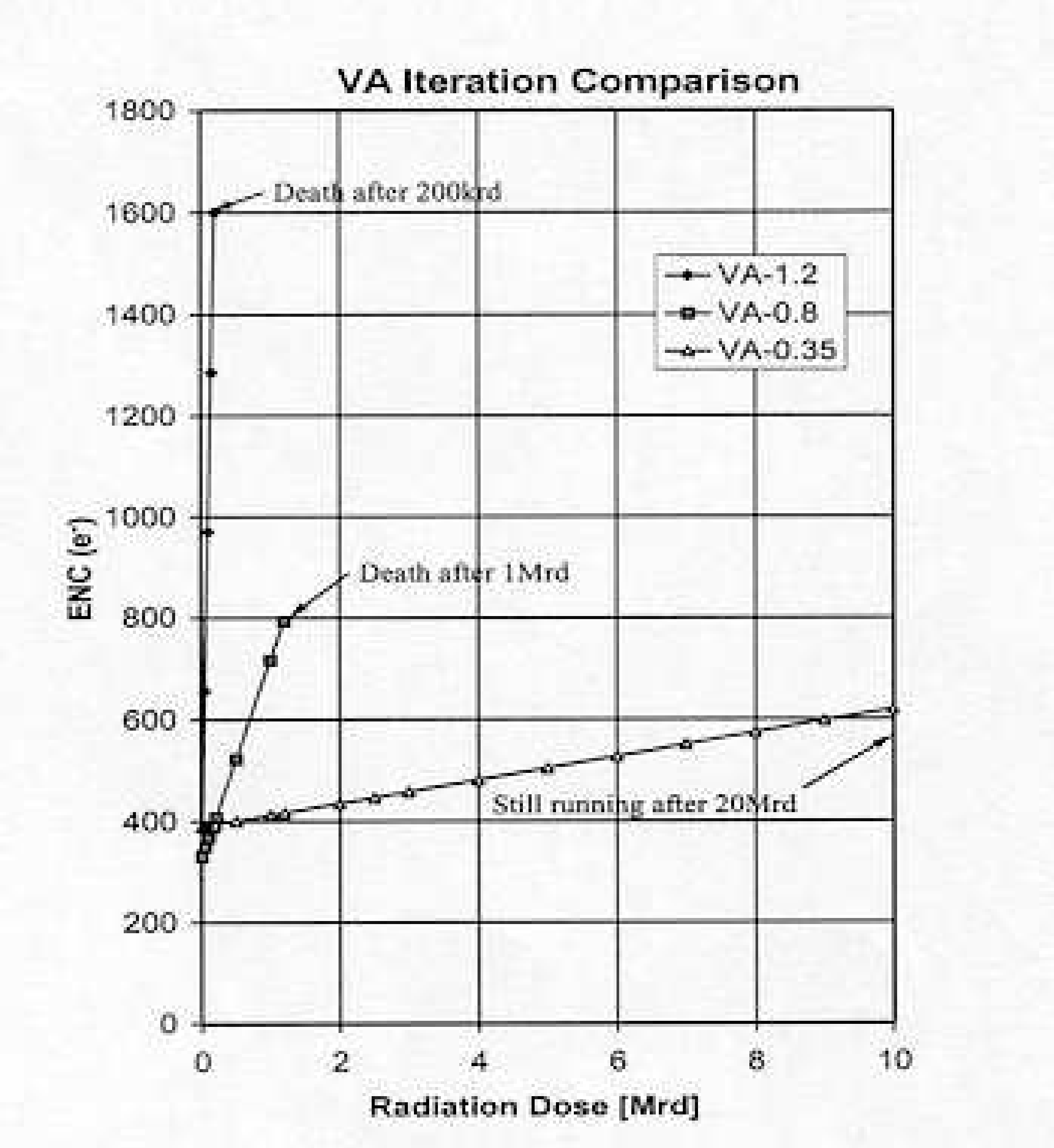
Figure 1: VA1 Architecture

VA_Rich is similar, but with individual output for each Track & Hold.

Radiation tolerance of Viking (VA) chips.

BELLE SVD uses the Viking VA1 chip, but needs radiation tolerance.
They radiation tested VA1 with different AMS technologies:

1.2 μm (VA1), 0.8 μm, and 0.35 μm (VA1_prime)



$\Longrightarrow$ BELLE SVD2 will use VA1_prime (0.35 μm AMS).

Preliminary summary on front-end amplifier chips

Viable options:

- **Viking**
  Visit to producer revealed capability and willingness to modify existing chips to our needs. Technology is in-house.

  Radiation hardness (0.8 μm or 0.35 μm AMS) demonstrated.

  Option 1: VA_rich in VA1_prime technology, higher dynamic range
  Option 2: As 1, plus analog trigger sum on chip to be used for L1.

- **HAL25**
  Unmodified copy of HAL25 with 512 channels/sector.
  L1 trigger not possible.

Read-out scheme

Read-out system must:
– Transfer data from FE electronics $\longrightarrow$ Receiver
– Digitize data and store in digital memory
– Data reduction if necessary
– Interface to ALICE DAQ

Same system should handle:
– Trigger $\longleftrightarrow$ FE electronics
– Slow controls of FE and hybrids
– Monitoring of Si detector, FE and hybrids
– Calibration, testing etc.

VA and HAL25 style chips deliver analog, serial data output.
Good signals max. 2–3 m cable (cf. transfer speed and acceptable noise).
In ALICE typical minimum distance to 'free' space is $\approx$ 5 m.

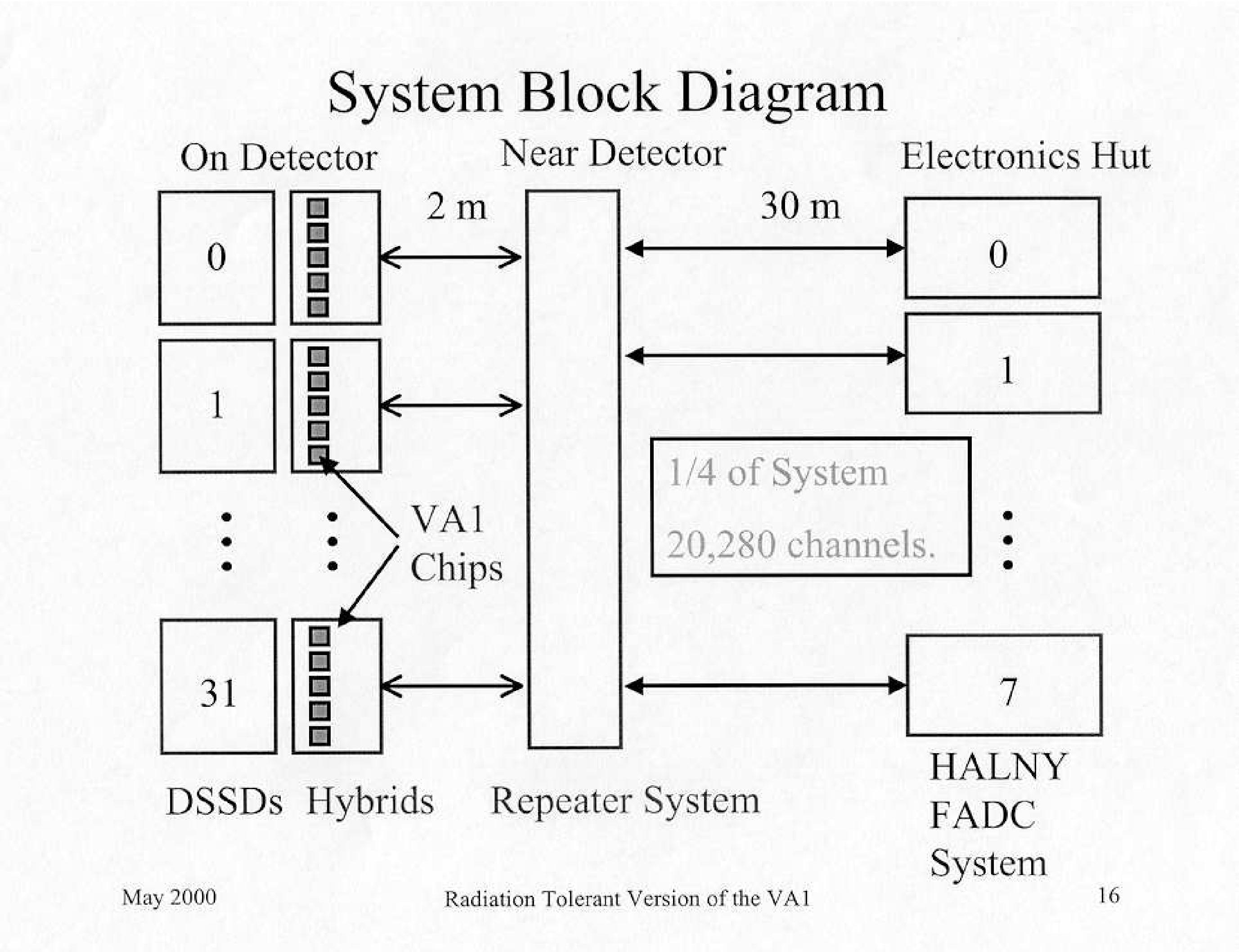
Suggested architecture:

- Hybrid with only FE chips and few passive components
- Analog signal receiver/repeater on/close to detector
- Receiver/digitizer/control card in VME

Option: Digitizer (ADC) on receiver card on detector, digital transfer.

Many examples of successfull read-out systems for Viking chips.

BELLE SVD read-out system:



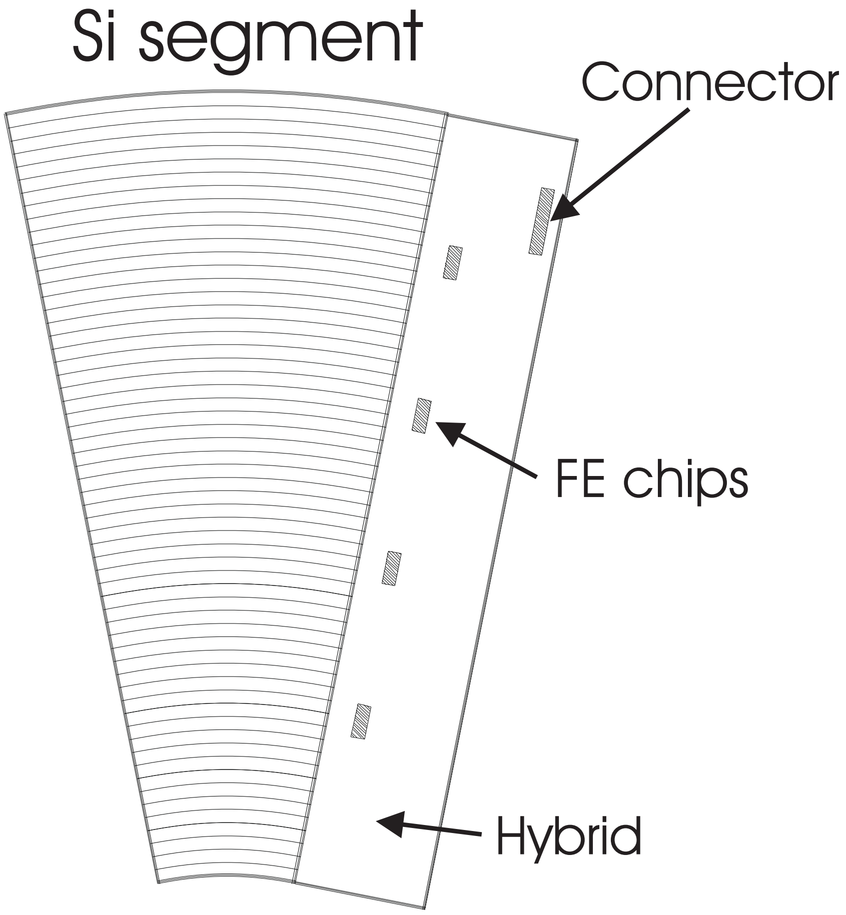
PHOBOS (RHIC) has similar architecture, except repeater system is 'trivial' buffer amplifier.

We would put Repeater System inside the detector assembly ... ⟶

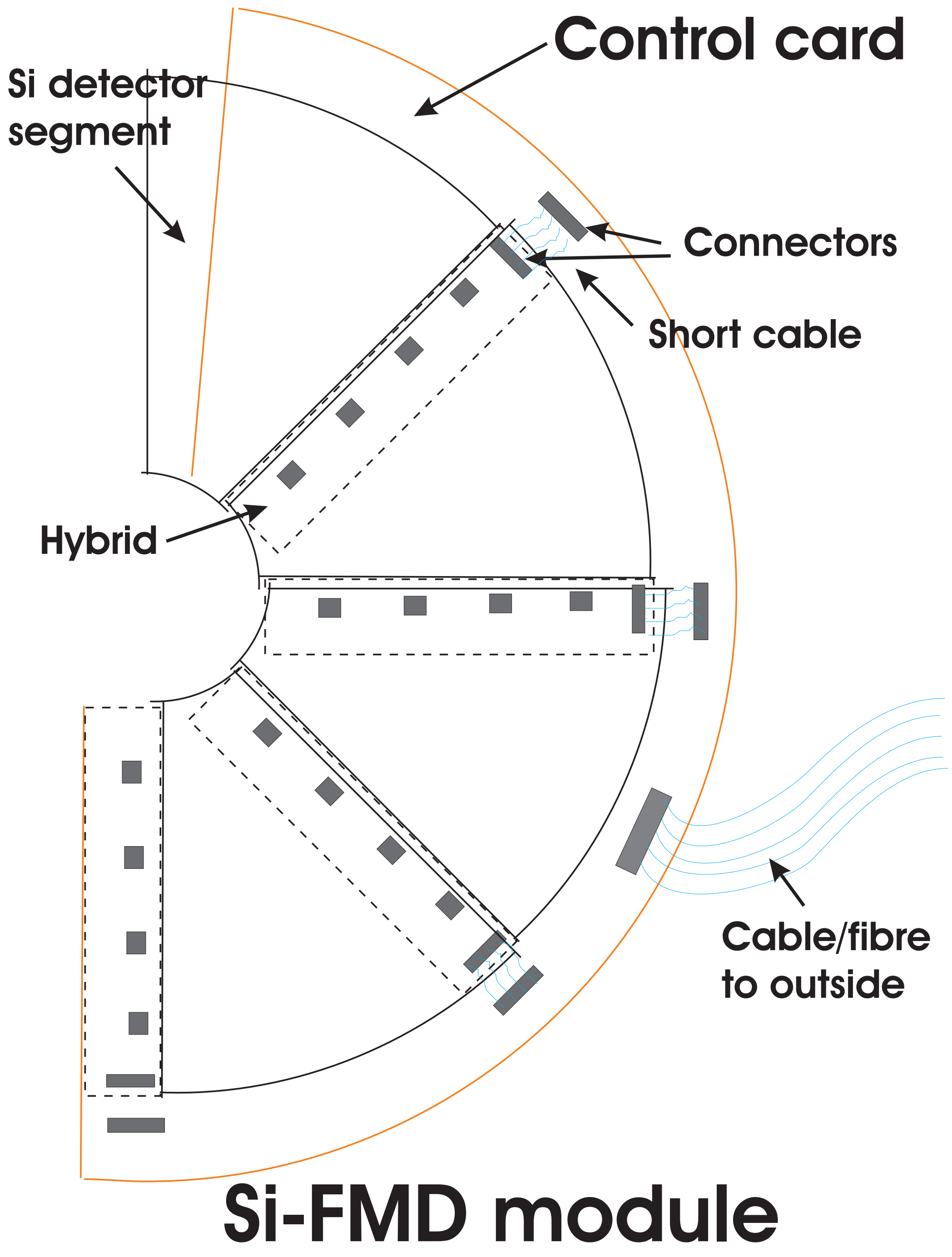
Hybrids

Hybrids are PC boards (often ceramics), integral part of detector system.
Suggest elongated hybrid along long side of Si detector:

– Mechanical support of Si detector
– Holds FE amplifier/trigger chips
– Holds passive components for signal and power distribution
– Pads for bonding of Si strips
– Connector for cable with for data read-out and chip controls.



Sketch of possible Si-FMD assembly with control/receiver/repeater system on PC card right behind detector.



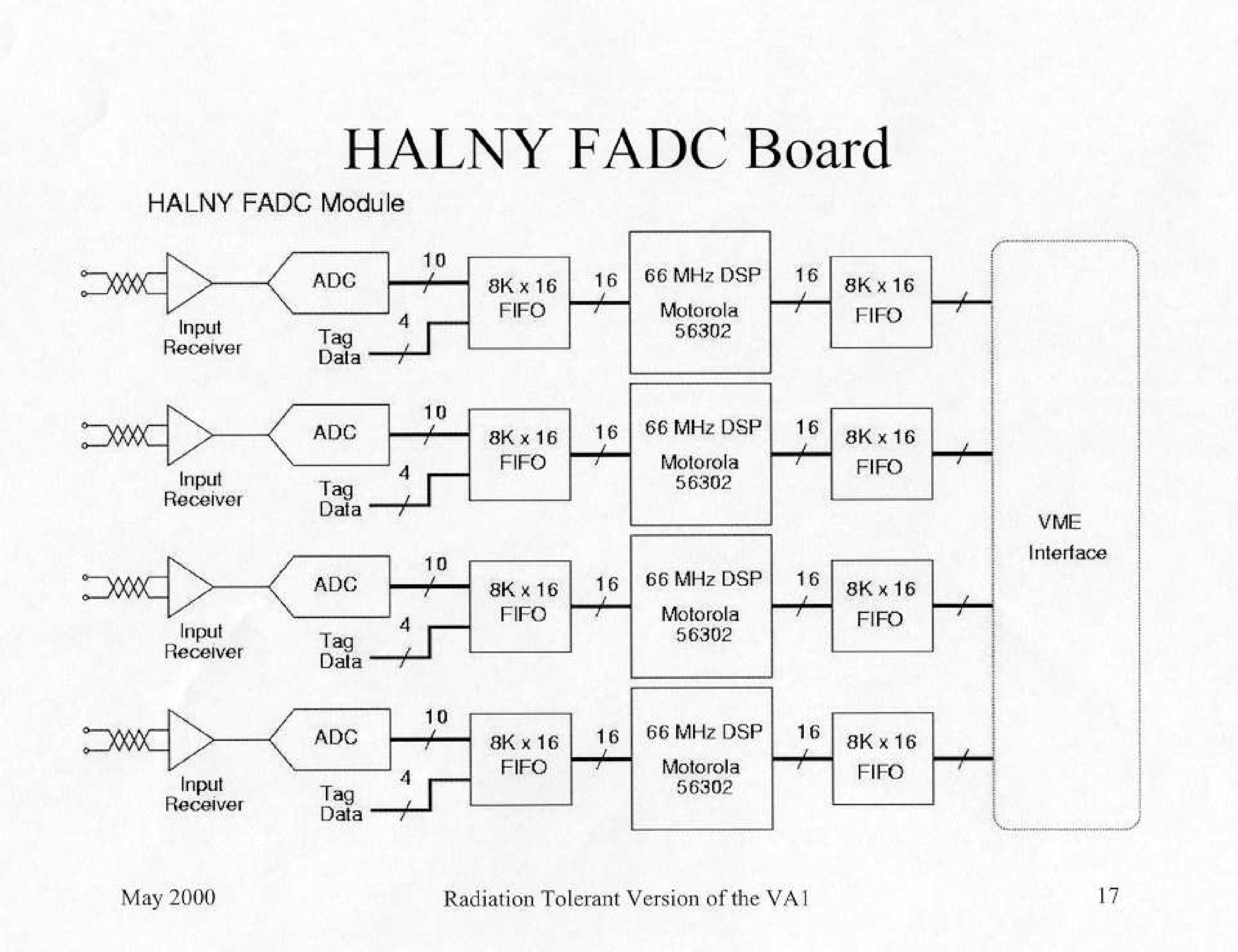
Receiver modules for read-out, monitoring and control of VA systems.

PHOBOS also has powerful Front-End Controller module with read-out + all control functions for the VA's.

HALNY is a general purpose VME system ($\approx$ SCIROCCO), developed for BELLE in Cracow.

SCIROCCO was used in DELPHI and commercialised by CAEN.

We should be able to can copy or buy.



The Viking (VA) electronics option

IDEAS (Norway) can deliver:

1. Front-end preamp/shaper chip of the Viking type:
   (a) modified VA_Rich for Si-FMD specs w/o L1 trigger
   (b) modified VA_Rich with analog sum trigger for L1
2. Hybrid design, production and chip mounting
3. Simple controller and read-out system to specifications
4. Test equipment, based on PC and LabVIEW.

Very approximative cost to IDEAS (based on 16,000 channels):

1. (a) 80 kCHF
   (b) 130 kCHF
2. 100 kCHF
3. 60 kCHF
4. 10 kCHF

Very preliminary power budget (one inner+outer wheel):
FE chip 1 mW/channel $\Longrightarrow$ 5 W
+ controls, analog signal drivers etc. Total $\approx$ 10 W

Summary

Since last FMD meeting (Feb 2001), we have investigated electronics solutions based on commercial Viking VA front-end chips.

We have also looked a bit more at the trigger and read-out aspects.

Two solutions appear:

- **Viking** (baseline):
  – IDEAS can modify the classic Viking (VA) preamp/shaper chips in radiation tolerant technology (0.8 μm AMS, verified to 1 Mrad) to include analog trigger sum for L1 triggering.

  – The chip is adaptable to our detector specifications (with e.g. 128 channels/sector, 15,000 total).

  – A 0.35 μm AMS chip can be made, but at higher price.

  – A VA system is also possible without trigger at a slightly lower cost.

  – IDEAS is capable and willing to enter hybrid design/production and first level read-out system. Test setup exists.

  – The HEP community has lots of experience with Viking systems.

  – Highly recommended by both PHOBOS and BELLE SVD, who may also help to provide full read-out system.

- **SSD copy** (alternative):
  – A system without L1 trigger and with 512 channels/sector (60,000 channels total) is possible based on the HAL25 chip.
  – This system would be a direct copy of ALICE SSD, only with a redesigned hybrid layout.