NBI

Towards the choice of Si-FMD electronics

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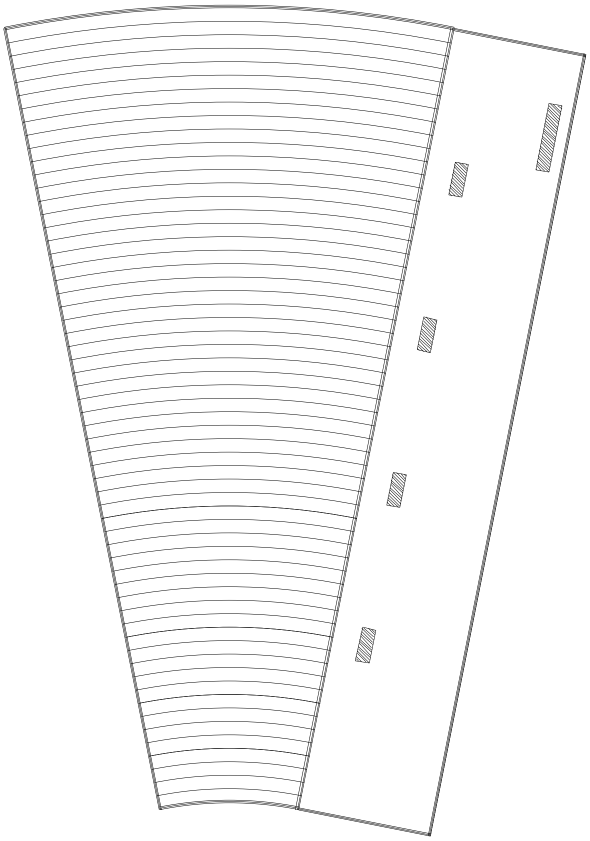
Table of Contents

Summary of Si detector characteristics

Channels per sector	32	64	128	256	512
Strip areas [cm^2]	0.8–3.7	0.4–1.8	0.2–0.9	0.1–0.5	0.05–0.23
Strip capacitances [pF]	32–131	19–66	12–36	8–22	7–13
Occupancies [# particles/strip]	4–22	2–11	1–5	0.6–3	0.3–1.3

Capacitance $\approx 34\mathrm{pF}/\mathrm{cm}^2 + 5\mathrm{pF}$
1 mip (300 μm) = 3.6 fC = 22,400 e^-



Summary of trigger requirements

Bunch crossing (BC) 25 ns / 50 ns

Trigger level	Time	Detectors	Comment
Pretrigger to TRD	BC + 100 ns	T0, V0 ?	
L0 accept	BC + 900 ns	T0, V0, Dimuon	deadtime free
L1 accept	BC + 5.2 μs	ZDC, FMD, TRD	abort if absent
L2 accept/reject	BC + 88 μs	nobody so far	abort on reject readout on accept
L3 daq	before ev.build.		
L4 daq	after ev.build.		

Requirements for front-end electronics

Depends on:

— Detector segmentation (capacitance, occupancy)
for 128 channels per sector: $C \leq 36pF$, $n \leq 5$
— Participation in trigger (L0, L1, ...)

	L0	L1	No trigger / L2
Sample & Hold Event pipe-line	40 MHz, no deadtime Continuous sampling Latch on L0	Latch on L0 signal no	Latch on L0 signal no
Peaking time or	$\approx$ 25ns	$\approx 1\mu$s $\approx$ 25ns+1μs pipe	$\approx 1\mu$s $\approx$ 25ns+1μs pipe
Trigger sum	Very fast analog sum continuously, 40 MHz $<$ 500ns latency	analog or digital sum $< 5\mu$s latency	no / analog or digital no / $< 80\mu$s
Readout or Digitize	Serial from pipe on chip or on hybrid	$< 5\mu$s serial on chip or on hybrid	serial on chip or on hybrid
Capacitance Dynamic range Noise Radiation hard	$\leq$ 66 / **36** / 22 / 13 pF (64 / **128** / 256 / 512 ch) 0 – 110 / **55** / 27 / 13 mips (64 / **128** / 256 / 512 ch) $\leq$ 0.1 mips (2,200 e$^-$) $\geq$ 200 krad		

Survey of some front-end chips

Survey of some front-end chips

Front-end chip	DELTA	DeltaStream	VA1_prime	ALICE128	HAL25
Experiment	CMS	CMS	Belle	ALICE	ALICE
Detector	Preshower	Preshower		ITS SSD	ITS SSD
Peaking time	25 ns	25 ns	0.3-1 μs	1.4-2 μs	1.2-2.2 μs
Channels	32	36	128	128	128
Dynamic range	0-400 mips	0-400 mips	$\pm$ 10 mips	$\pm$ 13 mips	$\pm$ 14 mips
	0-50 mips	0-50 mips	0-20 mips	0-26 mips?	0-28 mips?
Input capacitance	$<$ 60 pF	$<$ 60 pF	large	$<$ 20 pF	$<$ 20 pF
Noise	640e+33e/pF	1100e+35e/pF	180e+7.5e/pF	290e+8e/pF	207e+10e/pF
@ 30 pF	1630 e^-	2150 e^-	405 e^-	530 e^-	507 e^-
Memory/pipe	no	1 event S/H	1 event S/H	1 event S/H	1 event S/H
Read-out	analog	analog	analog	analog	analog
	parallel	serial	serial	serial	serial
	25 ns	50 ns/ch	100 ns/ch	100 ns/ch	100 ns/ch
Read-out time	25 ns	1.8 μs	12.8 μs	12.8 μs	12.8 μs
			3.2 μs/32ch		3.2 μs/32ch
Trigger on chip	no	no	no	no	no
Trigger on hybrid	L0 ?	L0 no	L0 no	L0 no	L0 no
	L1 yes	L1 yes	L1 ?	L1 ?	L1 ?
	L2 yes	L2 yes	L2 yes	L2 yes	L2 yes
Technology	DMILL/sub-μ	DMILL	0.35 μ	1.2 μ	0.25 μ
Rad. hard	yes	yes	yes	no	yes
Possible use	L0	–	NT, L1?	–	NT, L1?

Survey of some front-end chips (cont)

Front-end chip	DELTA+PACE	PASCAL	Carioca	APV25	SCTA	ABCD
Experiment	CMS	ALICE	LHCb	CMS	ATLAS	ATLAS
Detector	Preshower	ITS SDD	Muon det	Tracker	Tracker	Tracker
Peaking time	25 ns	50-60 ns	14-25 ns	50 ns	25 ns	25 ns
Channels	32	64	16 ?	128	128	128
Dynamic range	0-400 mips	0-12 mips	few mips?	0-10 mips?	few mips?	few mips
	0-50 mips					
Input capacitance	< 60 pF	< 20 pF	< 200 pF	< 25 pF	< 20 pF	< 20 pF
Noise	640e+33e/pF	210e+3e/pF	450e+27e/pF	270e+38e/pF	720e+33e/pF	559e+35e/pF
@ 30 pF	1630 e^-	300 e^-	1260 e^-	1410 e^-	1710 e^-	1609 e^-
Memory/pipe	160 events	256 events		192 events	112 events	132 events
Read-out	analog	digitized	binary	analog	analog	binary
	serial	parallel		serial	serial	
	50 ns/chan.	62 ns/word		50 ns/chan.	25 ns/chan.	
Read-out time	4.8 μs/3 ev	1.4 μs/ev			3.2 μs/ev	
	3.2 μs/2 ev	358 μs		7 μs	358 μs	
Trigger on chip	no	no	no	no	no	no
Trigger on hybrid	L0 before PACE	L0 no		L0 no	L0 no	L0 no
	L1 yes ?	L1 no ?		L1 no	L1 yes	L1
	L2 yes	L2 no ?		L2 yes	L2 yes	L2
Technology	DMILL/sub-μ	0.25 μ	0.25 μ	0.25 μ	DMILL	DMILL
Rad. hard	yes	yes	yes	yes	yes	yes
Possible use	NT, L0?, L1?	NT, L1(mod?)	–	–	L1?	–

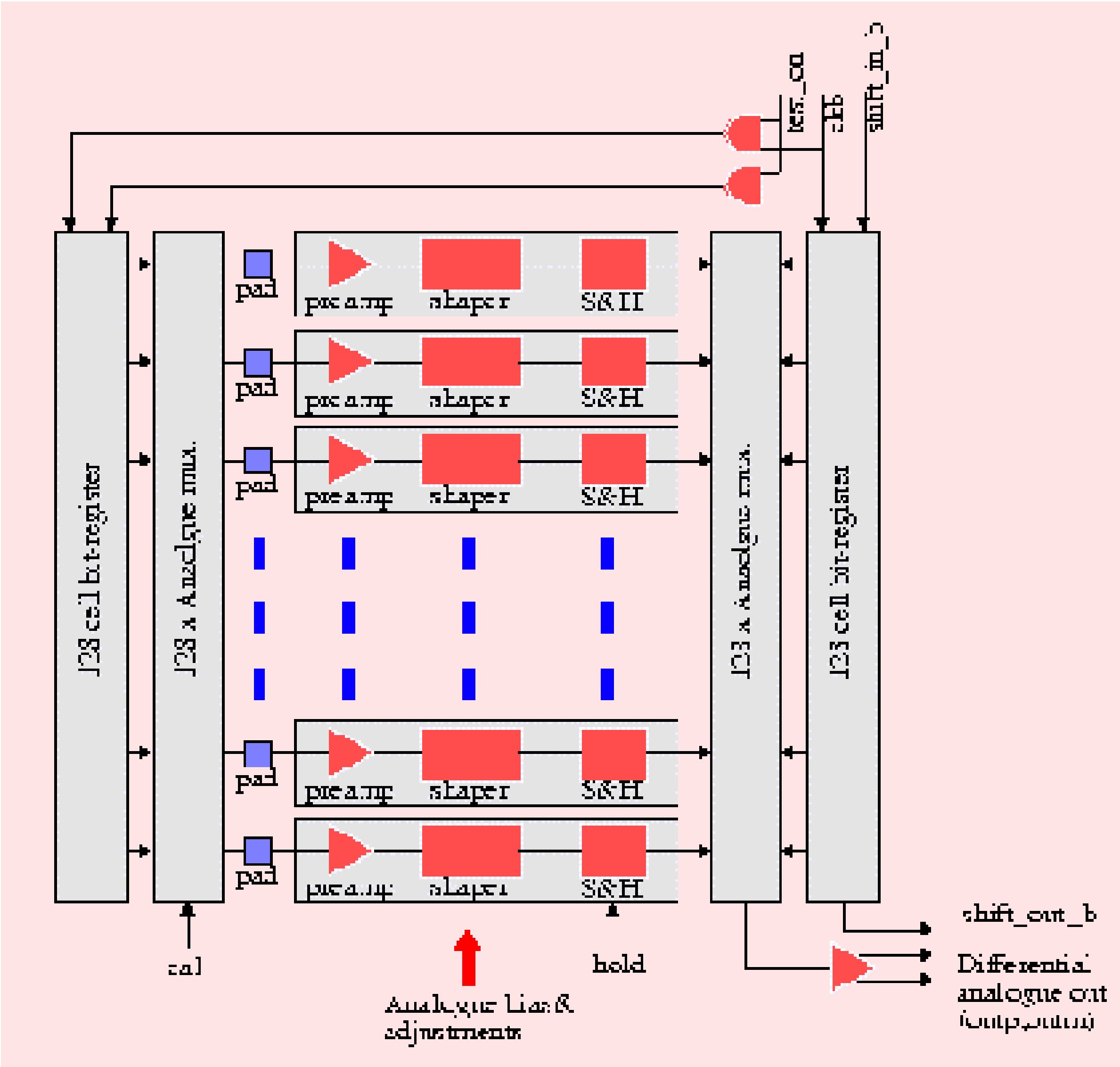
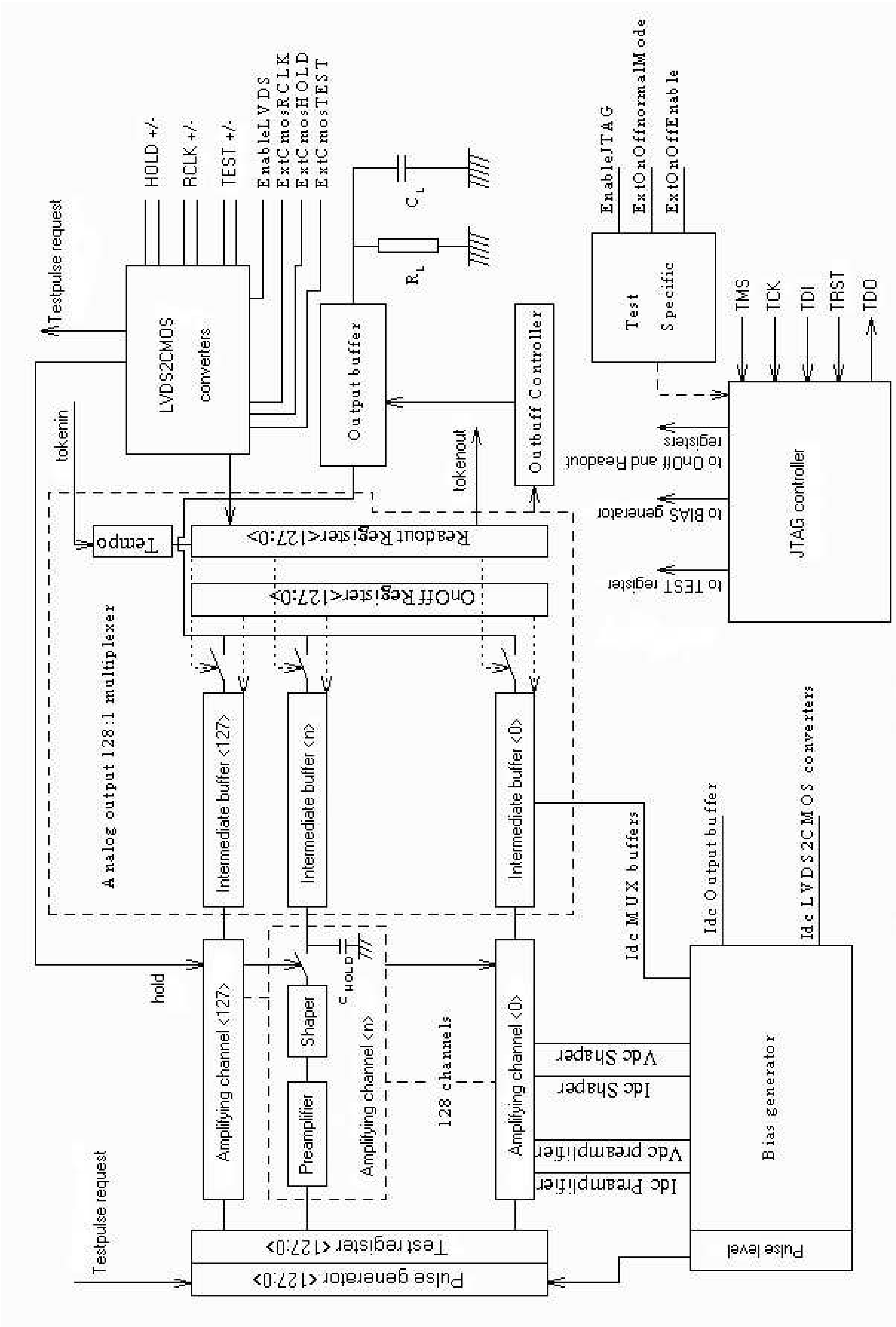


Figure 1: VA1_prime2 Architecture



Block diagram of ALICE128C

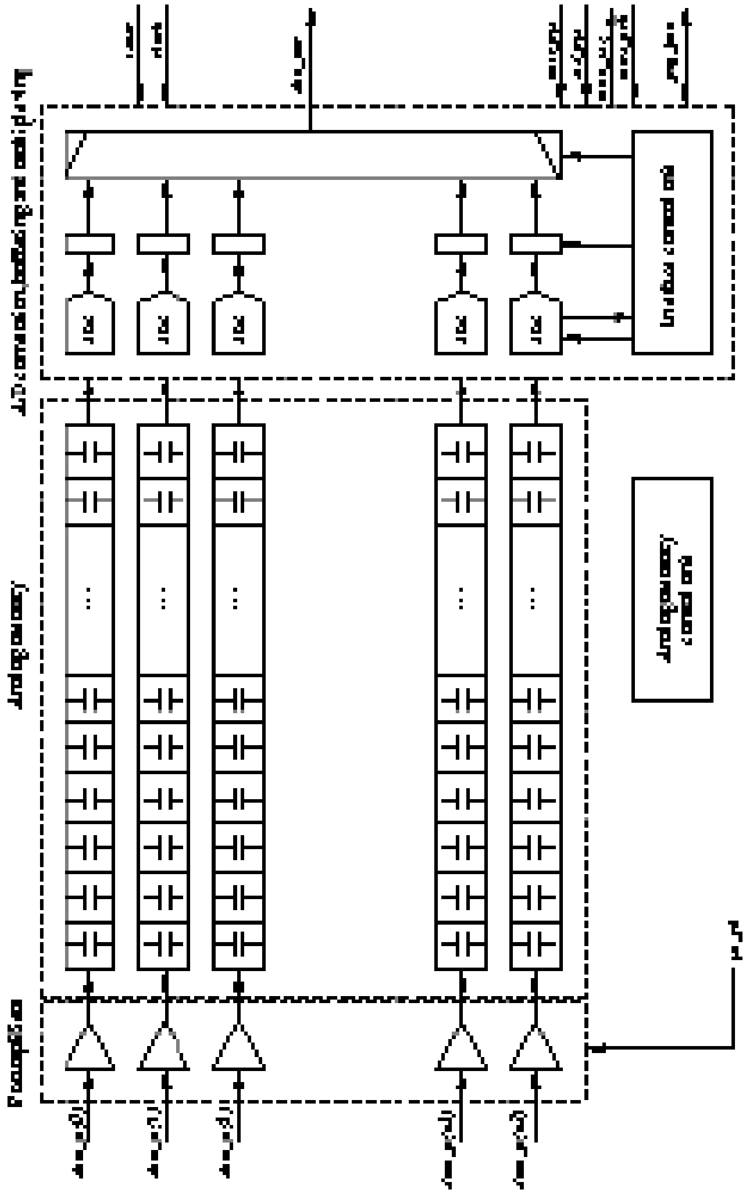
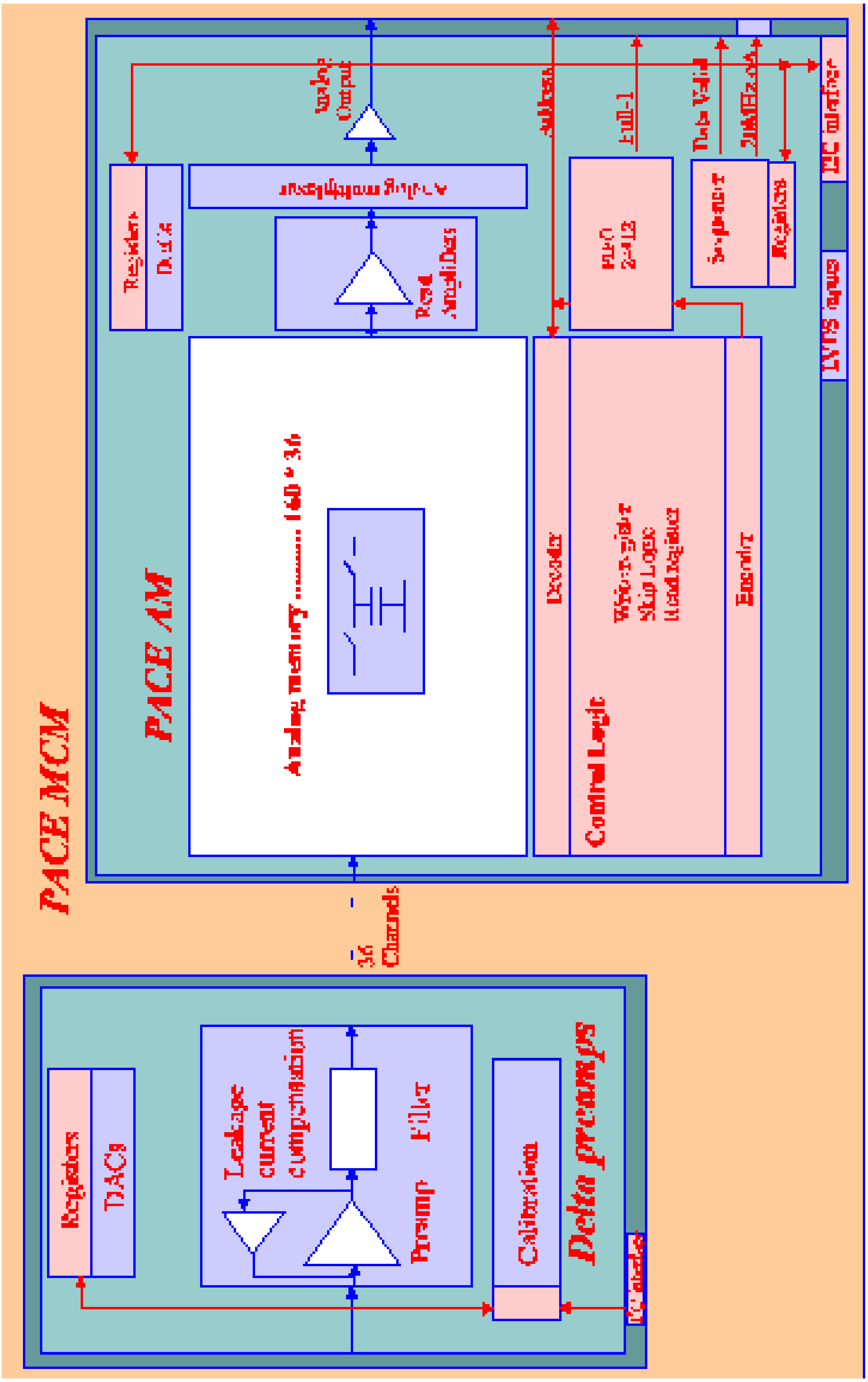


Figure 3.35: The PASCAL architecture.


PACE MCM
PACE AM
Analog memory .... 160 * 36
Control Logic
Decoder
Encoder
Read Amplifiers
Registers
DACs
36 Channels
Delta preamps
Leakage current compensation
Preamp
Filter
Calibration

Preliminary conclusions

1. # strips/sector ≥ 128
2. L0 triggering very difficult with Si, must be done by T0 and V0
3. L1 triggering not obvious with existing electronics
4. Digitization on chip/hybrid is the aim (easier cabling, readout)

Specifications for the ideal electronics, assuming L1 trigger:

— Radiation hard: $\geq 200\text{krad}$
— Noise: $\leq 0.1\text{mips}$
— Capacitance: match maximum strip size
— Dynamic range: $0 - 10 * \text{n}$, switchable
— Peaking time: $0.8 - 1.2\mu\text{s}$, tunable
— On-chip S/H
— On-chip ADC
— Either: Fast, parallel read-out (form trigger sums on hybrid)
Or: Trigger sum on chip, separate out + serial readout
— Test + calibration circuits
— Simple slow controls
— Compatible with other ALICE subsystems: slow contr. + DAQ
— Early version for Si detector testing
— Affordable costs

Existing front-end candidates not ideal, but possibly adaptable:

- PACE:
  - complicated, not ALICE, but seems OK
  - can take large capacitances + occupancies
  - analog trigger formed during readout, on hybrid
  - can we use CMS ADC's and controls?
- HAL25:
  - nice and simple, ALICE SSD
  - need ≥ 256 channels/sector due to occupancies
  - analog trigger formed during readout
  - use is limited to 32 channels – or less, due to L1 latency
  - ADC's and contros on hybrid
- PASCAL:
  - very nice and compact, ALICE SDD
  - needs $\geq$ 512 channels/sector (low occupancy) or lower gain
  - ADC's on chip, fast digital readout
  - digital trigger formed during readout
  - problem with readout pointer needs chip modification
  - can we modify chip? (switchable gain, modified readout pointer)
- SCTA:
  - ATLAS chip not used by ATLAS
  - fast analog readout
  - should maybe be looked at again

Hybrid

- Form trigger on hybrid/module; analog/digital sum to trigger system
- Digitize full data on chip or on hybrid
- Transfer full data to DAQ serially per module, digital
- Controls
- Power etc.

How do we proceed?

We can

1. Specify, develop and produce own electronics.
   Warning: rad. hard cycle time $\approx$ one year
   Project must include: radiation hard solution, test samples, detailed schedule and cost
2. Modify existing chips.
   Collaborate with designers
   Common or separate production
3. Adapt Si design to existing chips.
   Common or separate production

Path 1. is interesting, but requires large resources.
We must not forget to include hybrid development, DAQ etc.

Path 2. is worth pursuing.
Could this be a more manageable engineering project?

Path 3. may be the only affordable way out.